|  |  |  |  |
| --- | --- | --- | --- |
| **nbit\_shiftreg Project Status (10/28/2017 - 20:31:30)** | | | |
| **Project File:** | Lab3.xise | **Parser Errors:** | No Errors |
| **Module Name:** | T\_flipflop | **Implementation State:** | Synthesized |
| **Target Device:** | xc3s500e-4ft256 | * **Errors:** |  |
| **Product Version:** | ISE 14.7 | * **Warnings:** |  |
| **Design Goal:** | Balanced | * **Routing Results:** |  |
| **Design Strategy:** | Xilinx Default (unlocked) | * **Timing Constraints:** |  |
| **Environment:** | System Settings | * **Final Timing Score:** |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Device Utilization Summary (estimated values)** | | | | **[-]** |
| **Logic Utilization** | **Used** | **Available** | **Utilization** | |
| Number of Slices | 1 | 4656 | 0% | |
| Number of Slice Flip Flops | 2 | 9312 | 0% | |
| Number of 4 input LUTs | 2 | 9312 | 0% | |
| Number of bonded IOBs | 4 | 190 | 2% | |
| Number of GCLKs | 1 | 24 | 4% | |

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| --- | --- | --- | --- | --- | --- | --- |
| **Detailed Reports** | | | | | | **[-]** |
| **Report Name** | **Status** | **Generated** | **Errors** | **Warnings** | **Infos** | |
| Synthesis Report | Current | Sat 28. Oct 20:26:36 2017 |  |  |  | |
| Translation Report |  |  |  |  |  | |
| Map Report |  |  |  |  |  | |
| Place and Route Report |  |  |  |  |  | |
| CPLD Fitter Report (Text) |  |  |  |  |  | |
| Power Report |  |  |  |  |  | |
| Post-PAR Static Timing Report |  |  |  |  |  | |
| Bitgen Report |  |  |  |  |  | |

|  |  |  |  |
| --- | --- | --- | --- |
| **Secondary Reports** | | | **[-]** |
| **Report Name** | **Status** | **Generated** | |
| ISIM Simulator Log | Out of Date | Sat 28. Oct 20:31:15 2017 | |

**Date Generated:** 10/28/2017 - 20:31:30